

2114  
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application No.: 10/084,105  
Filed: February 27, 2002  
Inventor(s):  
Andrew Phelps

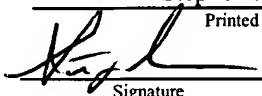
Examiner: Chu, Gabriel L.  
Group/Art Unit: 2114  
Atty. Dkt. No: 5181-97700

Title: A Memory Subsystem  
Including an Error  
Detection Mechanism for  
Address and Control Signals

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on the date indicated below.

Stephen J. Curran

Printed Name

  
Signature

December 7, 2004

Date

AMENDMENT; RESPONSE TO OFFICE ACTION OF  
SEPTEMBER 7, 2004

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

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**Technology Center 2100**

Dear Sir:

This paper is submitted in response to the Office Action of September 7, 2004, to further highlight why the application is in condition for allowance.